Claims

What is claimed is:

1. An auto-clamping circuit responsive to a reset signal for tying an input terminal of an integrated circuit to a definite voltage potential, the auto-clamping circuit comprising:

a conductive input line coupled to an input terminal; and

electronic switching means coupled between the input line and a voltage supply line, the electronic switching means effective for coupling the input line to the voltage supply line whenever a reset signal is asserted upon the electronic switching means.

2. The auto-clamping circuit as in claim 1, further comprising:

a voltage level maintaining means also responsive to the reset signal and also coupled between the input line and the voltage supply line, but weaker in its conductance capability than the electronic switching means, for holding the input line at a fixed voltage potential once the reset signal is de-asserted until driven by a signal applied to the input terminal.

3. The auto-clamping circuit as in claim 2, wherein the voltage level maintaining means is a circuit comprising:

a NAND logic gate having a first input coupled to the input line, a second input coupled to receive the reset signal, and an output coupled to any remaining portion of the integrated circuit; and

a transistor coupled between the input line and the voltage supply line, and having a gate terminal coupled to the output of the NAND gate.

4. The auto-clamping circuit as in claim 1, wherein the electronic switching means comprises a transistor coupled between the input line and the voltage supply line, and having a gate terminal coupled to receive the reset signal.

5. The auto-clamping circuit as in claim 4, wherein the reset signal is an active low signal, the transistor is an n-channel FET, and an inverter is coupled to the gate terminal of the transistor for inverting the reset signal.

6. The auto-clamping circuit as in claim 1, wherein the voltage supply line is at ground potential.

7. An auto-clamping circuit responsive to a reset signal for grounding an input terminal of an integrated circuit, the auto-clamping circuit comprising:

a conductive input line coupled to an input terminal;

a first pull-down transistor coupled between the input line and a ground, and having a gate terminal coupled to receive a reset signal, the pull-down transistor effective for discharging the input line to ground whenever the reset signal is asserted upon its gate terminal;

a NAND logic gate having a first input coupled to the input line, a second input coupled to receive the reset signal, and an output coupled to any remaining portion of the integrated circuit; and

a second pull-down transistor coupled between the input line and ground, and having a gate terminal coupled to the output of the NAND gate, the second pull-down transistor weaker in its conductance capability than the first pull-down transistor but effective for maintaining the input line at a fixed voltage potential once the reset signal is de-asserted until driven by a signal applied to the input terminal.